



An 87% Efficient Wireless Powered System Using Adaptively Controlled Active Rectifier for Smart Electronics

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I. INTRODUCTION

This paper presents an effective wireless power system (WPS) for powering smart electronics [1], including battery charging. To enhance the performance of the WPS, we have utilized an adaptively-controlled active rectifier matrix (AARM) that also helps to regulate the output voltage over a wide-range load variation. In addition, we proposed a digital compensation circuit that adjusts both turn-on and turn-off times of to compensate for delays of the comparator when it turns off and on. Then proposed WPS is implemented in a 0.18 μm process. The WPS can achieve 270 mW of the peak power while flowing 135 mA of the load current. The measured peak efficiency is 87% at 0.89 mW of the output power.

II. DESCRIPTION

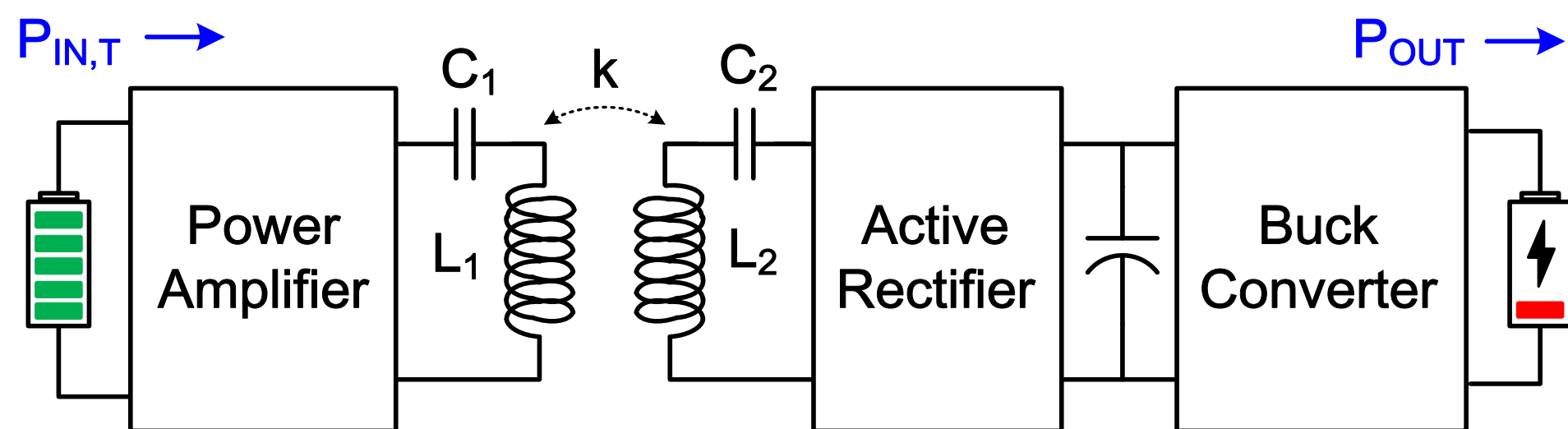


Fig. 1. Block diagram of the conventional WPS with a buck converter.

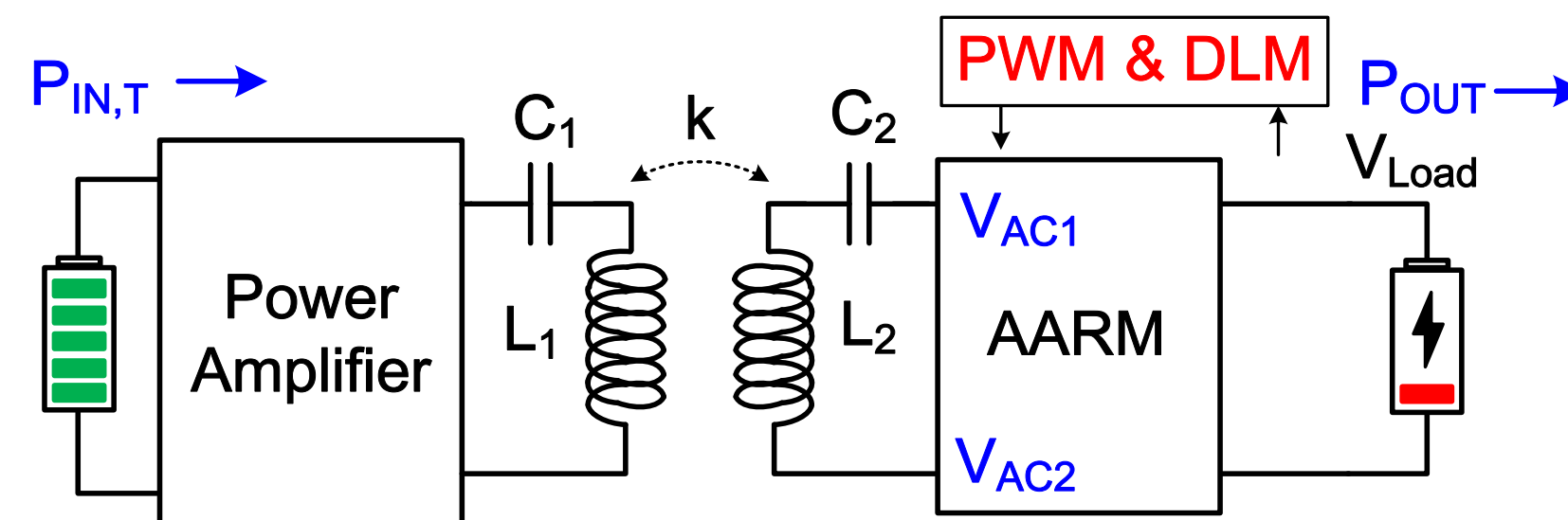


Fig. 2. Block diagram of the proposed WPS without using buck converter.

Fig. 1 shows the conventional WPS, it typically consists of a transmitter (TX) and a receiver (RX). There are two main controllers on the receiver side: an active rectifier for improving rectification efficiency and a DC-DC converter controlled by the output. In this scenario, we can express the total converter efficiency (η_T) as in [2, 3]

$$\eta_T = \eta_{AMP} \times \eta_{LINK} \times \eta_{RECT} \times \eta_{BUCK} \quad (1)$$

Fig. 2 shows the simplified block diagram of the proposed wireless powered system, and it consists of a power amplifier and the AARM. The AARM is controlled by the pulse width modulation (PWM) and dynamic load-current modulation (DLM). The AARM can be directly connected to the battery with the maximum available power. Hence, we can obtain the total efficiency by concerning only three essential stages of the proposed method as

$$\eta_{T,Pro} = \eta_{AMP} \times \eta_{LINK} \times \eta_{AARM} \quad (2)$$

Fig. 3(a) shows the schematic of AARM, and it mainly consists of a PMOS switch matrix (PSM), a load voltage regulator (LVR) with related drivers, and tuning comparators (TCM1,2). The related aspect of the PMOS switch matrix is defined as 2^n , where n can change from 0 to 7. Fig. 3(b) shows the variation of the input AC voltages of the AARM (V_{AC1} and V_{AC2}) during startup. In this interval, the tuning comparator TCM1,2 and the active diodes have yet to start then, V_{Load} is increasing due to the parasitic diodes of the S_{N1} and S_{N2} switches, which refers to the passive rectification. When the V_{Load} overcomes the threshold to supply the TCM1,2, the active rectification will be enabled as shown in Fig. 3(c).

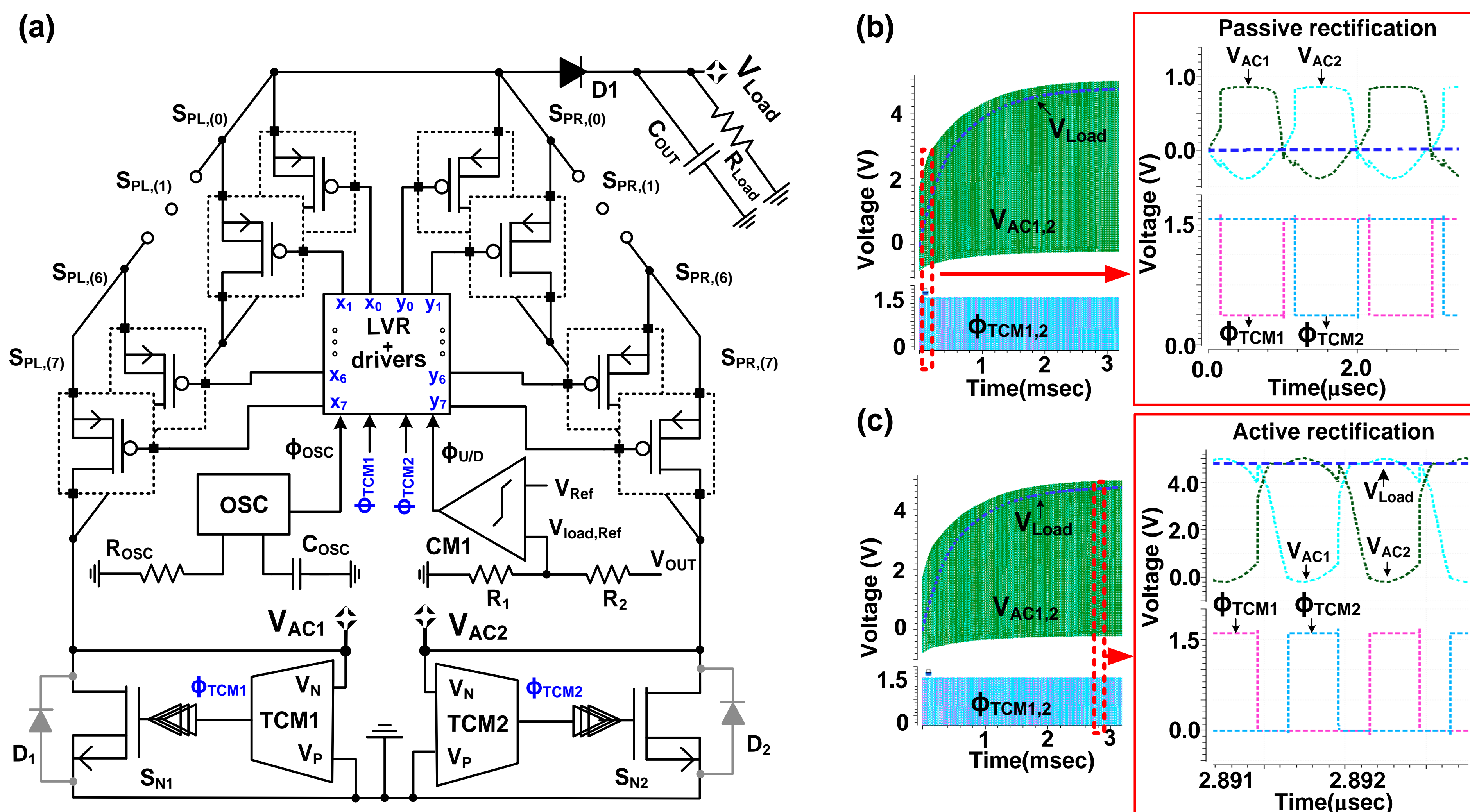


Fig. 3. (a) The overall system of the WPS and the simulated waveforms of illustrating (b) startup (c) steady-state operations.

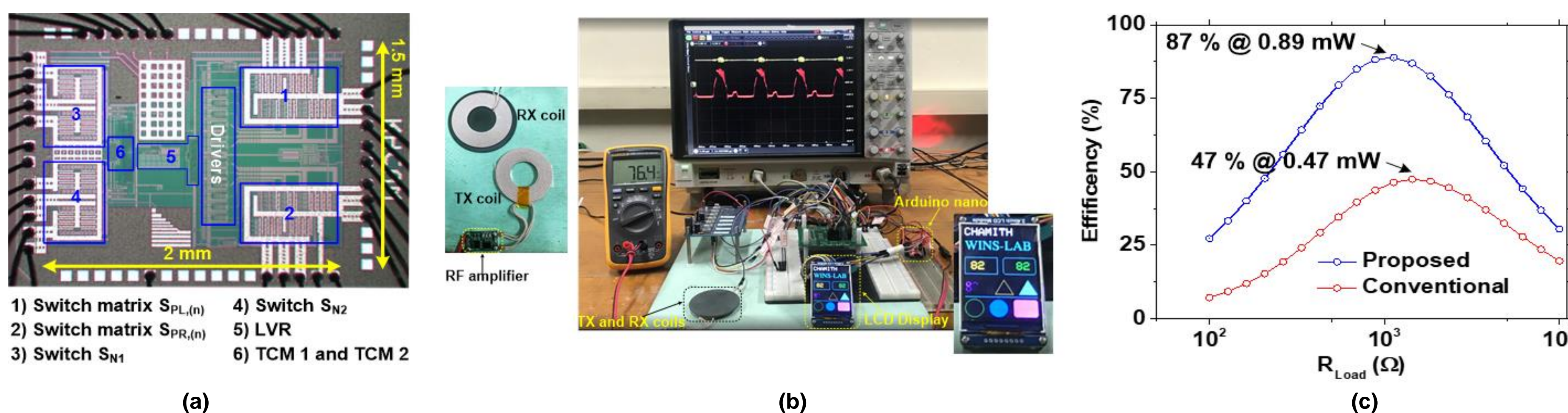


Fig. 4. (a) Die photograph of WPS, (b) measurement setup for powering LED display using the WPS, and (c) Variation of efficiencies as function of R_{Load} .

Fig. 4(a) shows the micrograph of the WPS consuming an active area of 3 mm², and it is mounted on the test board using the chip-on-board (COB) technique. Fig. 4(b) shows the measurement setup when powering LED display and Arduino nano. Fig. 4(c) shows the conversion efficiency as a function of load resistance for the proposed AARM and the conventional active rectifier. The WPS regulates output voltage V_{Load} at 3.2 V. The range of related input power is 0.03 – 0.9 mW. The maximum peak efficiency is 87%, while supplying 0.89 mW to R_{load} . The conversion efficiency of the active rectifier is around 47% which is much lower compared to proposed AARM.

Conclusion

Table. 1 can conclude the performance of this design. Our work can handle a relatively higher input range while V_{Load} is regulated depending on the R_{Load} demands. The overall R_{Load} range of our work is 0.1 – 100 k Ω , which is much higher than the other works [2, 3]. The proposed work achieves the highest load power $P_{Load} = 270$ mW at $I_{Load} = 135$ mA. Even in the low input power $P_{IN} = 0.98$ mW, our work can achieve a better peak efficiency of 87%.

References

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Acknowledgement

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Table 1. Performance comparison

	[2]	[3]	This work
Process	350 nm	180 nm CMOS	180 nm HV BCD
Type	RRR ^a	PLSK ^b	AARM
Cascaded Stages	4	5	3
Input range	3.6 V >	4 V	3 – 20 V
V_{Load}	3.6 V (regulated)	3.3 – 4.2 V	1 – 5 V (regulated)
Regulation method	PWM in TX	PWM in TX	PWM and DLM RX
Overall R_{Load} range	-	0.2 – 1 k Ω	0.1 – 100 k Ω
P_{Load} max	102 mW	180 mW @ $I_{Load} = 40$ mA	270 mW @ $I_{Load} = 135$ mA
Peak Efficiency	92% @ $P_{OUT} = 180$ mW	92.6% @ $P_{OUT} = 60$ mW	87% @ $P_{IN} = 0.98$ mW

^aReconfigurable resonant regulating, ^bPulsed load-shift keying